

A SMART VISION SYSTEM-ON-A-CHIP DESIGN BASED ON PROGRAMMABLE NEURAL PROCESSOR INTEGRATED WITH ACTIVE PIXEL SENSOR

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Abstract

A low power smart vision system based on a large format (currently 1Kx1K) active pixel sensor (APS) integrated with a programmable neural processor for fast vision applications is presented. The concept of building a low power smart vision system is demonstrated by a system design, which is composed with an APS sensor, a smart image window handler, and a neural processor. The paper also shows that it is feasible to put the whole smart vision system into a single MCM chip in a standard CMOS technology.

This smart vision system on-a-chip can take the combined advantages of the optics and electronics to achieve ultra-high-speed smart sensory information processing and analysis at the focal plane. The proposed system will enable many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics. Future applications will also include scientific sensors such as those suitable for highly integrated imaging systems used in NASA deep space and planetary spacecraft.

1. Low Power Smart Machine Vision System

Figure 1 shows a system diagram of the proposed smart vision system. The functional blocks include: (a) an active pixel sensor, (b) a smart image window handler, (c) a programmable neural processor, and (d) a host interface and timing control card. The APS is used as the optical sensing array in the system. The smart window handler manipulates the APS image data and provides the windowed image for the neural processor. The neural processor is programmed to perform various vision tasks in high speed due to its massively parallel computing structures and learning capabilities. The host computer through host interface and timing control card controls the APS sensor, the smart image window handler, and the programmable neural processor. The output image or vision science data will be displayed by the host computer.

It is feasible to build the proposed smart vision system in a single CMOS chip. This smart vision system on-a-chip can take the combined advantages of the optics and electronics to achieve low-power high-speed smart sensory information processing and analysis at the focal plane. The proposed system will enable many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics. Future applications will also include scientific sensors such as those suitable for highly integrated imaging systems used in NASA deep space and planetary spacecraft.

The following sections describe technical details of each building block of the proposed smart vision system and also show the feasibility to put the whole system into a single chip in a standard low power CMOS technology.

2. CMOS Active Pixel Sensor

A low power CMOS APS camera-on-a-chip has been developed for producing imaging systems that can be manufactured with low cost, low power, and with excellent imaging quality [1].

Charge-coupled devices (CCDs) are currently the competing technology for image sensors. However, CCDs cannot be easily integrated with CMOS without additional fabrication complexity. In addition, CCDs require two-order-of-magnitude higher power dissipation than that of APS. The CCD does not have the windowing capability to provide the input data to the neural processor. On the other hand, an APS imager does not have the above limitations and it is the suitable candidate for the proposed smart vision system.

The 1Kx1K APS is used as the optical sensing array and integrated with the neural processor to build the smart vision system for high definition vision applications. A low power 1Kx1K CMOS APS (operate from a +3.3 V supply) using 0.55 μ m n-well process was designed and characterized at JPL. Testing results show that the large format APS with small feature size (10 micron pixel pitch) is capable of excellent imaging performance.

A block diagram of the 1Kx1K APS chip architecture and its chip photo are shown in Figure 2. It contains a 1024x1024 photodiode or photogate pixel array and 1024 parallel 10-bit singles-slope ADC. The 10-bit decoders are controlled by input clocks to supply the row address and column address for analog or digital mode operation of the chip. The analog outputs are VS_OUT (signal) and VR_OUT (reset), and the digital outputs are D_out0 to D_out9. The analog and digital readout chains are separated by the pixel array. Each imager can be operated in analog or digital readout mode..

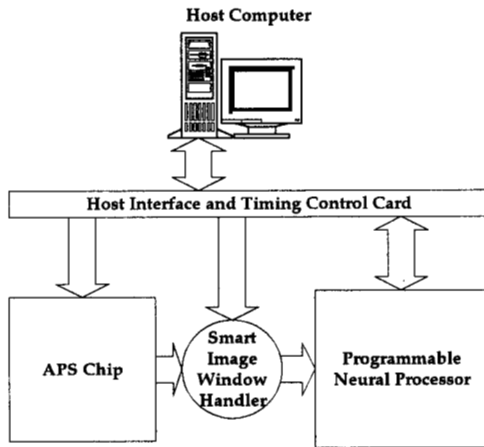


Fig. 1. A system diagram of the smart vision system.

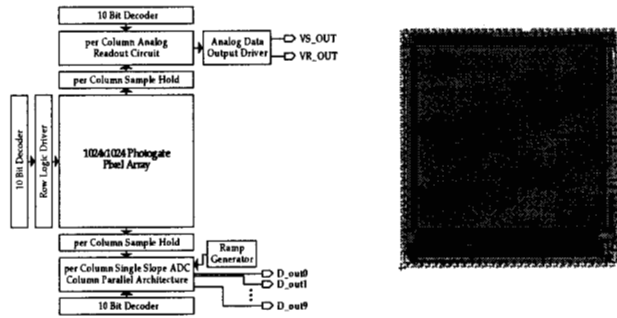


Fig. 2. Block diagram and chip layout of 1Kx1K CMOS APS.

3. Smart Image Window Handler

The APS images described in the previous section are capable of providing $m \times m$ sub-window image data to neural processor. However, the neural processor requires the input data in the format of $m \times m$ sub-window which shift in x rows and y columns basis through the whole image, where x and y are integer ranged from 0 to $n-1$. Thus, $(n-m+1) \times (n-m+1)$

sub-windows per frame are required for a $n \times n$ APS with a window shifting in 1 row and 1 column basis. In this case, the frame time of the APS chip as well as the system will be much longer than the frame time that the APS chip is running in the row by row output mode. The smart image window handler can solve this difficulty. The smart image window handler is designed for the interface between the APS chip and neural processor to achieve a fast frame time.

4. Programmable Neural processor

A programmable neural processor based on optimization cellular neural network (OCNN) has been used as a front-end sensory information processor to provide high throughput real-time computing power at neighborhood of the APS sensory circuit. The OCNN neural processor is programmable to perform various vision functions at very high speed in VLSI. Moreover, the OCNN architecture is a locally connected, massively paralleled computing system with simple synaptic operators so that it is very suitable for VLSI implementation. A compact VLSI OCNN neural processor is able to provide a powerful computing engine for the smart vision system. Both high data bandwidth and high performance computation are required for various vision functions. Incorporating the OCNN neural processor into the proposed vision system offers orders-of-magnitude computing performance enhancements for on-board real-time vision tasks.

4.1. Neuroprocessor Architecture and Features

The OCNN proposed for the vision system is an improved version of the original Cellular Neural Networks (CNN). Since its original publication by Chua and Yang [3,4] in 1988, the CNN paradigm has evolved rapidly and provides a unified framework for many computation-intensive applications such as signal processing and optimization. The CNN has been proved to be universal as the Turing machine [5]. As shown in Figure 3, the OCNN is a multi-dimensional array of mainly identical cells, which are dynamic systems with continuous state variables and locally connected with their local cells within a finite radius. Figure 3 also shows the model of the OCNN neuron $C(i,j)$. Many OCNN functions have been verified via system simulation. These functions include noise filtering, isolated pixel elimination, hole

filling, morphological operations, image enhancement, edge detection, connected component detection, feature extraction, motion detection, motion estimation, motion compensation, object counting, size estimation, path tracking, collision avoidance, minimal and maximal detection, etc. . The operation for different applications depends primarily on the coefficients of the templates and the procedure to apply them. A template includes the information for synapse weights, threshold values, and boundary conditions.

The OCNN design is targeted for smart vision system, it has four more significant features than the basic CNN:

(A) Optimal Solutions of Energy Function:

Under the mild condition [3], a CNN autonomously finds a stable solution for which the Lyapunov function of the network is locally minimized. To improve the local minimized energy function of the basic CNN, the annealing capability is included to accommodate the applications in which the optimal solutions of energy function are needed. Hardware annealing [6] is a highly efficient method of finding optimal solutions for cellular neural networks.

(B) Multiple Layers with Embedded Maximum Evolution Functions:

In the original CNN every pixel is represented by one neuron. In the OCNN every pixel can be represented by multiple neurons which form a hyperneuron and execute the maximum evolution function for various profile selections or the multi-sensor data synergy.

(C) Digitally Programmable Synapse Weights: To improve the fixed synapse weights of the basic CNN, the digitally programmable synapse weights are designed for the OCNN to accommodate the applications, which require programmable pre-determined operators.

(D) High-speed Parallel External Image I/O:

To improve the data I/O bandwidth of the basic CNN, an APS sensor is integrated with the OCNN to accommodate the applications, which require high-speed parallel image I/O.

The OCNN can be used as a front-end sensory information processor with the APS to provide high throughput real-time computing power at neighborhood of the sensory circuit. The OCNN operation theory, architecture, design and implementation, prototype chip, and system applications have been investigated in detail and presented in the references [2,8].

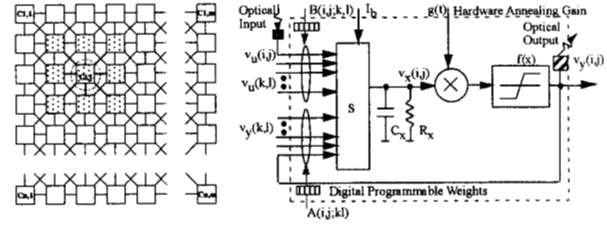


Fig. 3 OCCN Array and Processor Element Design.

An OCNN unit consists of a core neuron cell, synaptic weights, input/output circuits, and digital interface. To construct a complete OCNN, a multiple of the units can be arranged in an n-by-m rectangular grid with appropriate interconnections. Building blocks of the OCNN are briefly described in the following:

Programmable synapses: The digital programmable synapse is realized using a binary-weighted current source array. Programmability of -3.75 to 3.75 for each synaptic weight is provided. This synaptic weight function can achieve 5-bit programmability and a resolution of higher than 8 bits.

Transimpedance multiplier: The hardware annealing is performed by the pre-multiplication of the state v_{xij} by the gain control function g before the nonlinear function $f(x)$ takes place. The basic element of the proposed circuit is the double-MOS differential resistor operating in triode region

Summing circuit: If the summation of the weighted currents from the neighboring cells is carried out directly in the transimpedance multiplier, the value of resistance R_x is inversely proportional to the gain-control voltage V_c . In order to accommodate a constant R_x , the constant input impedance current inverter is used at the input stage of the multiplier.

Nonlinear function: The circuit for the nonlinear function $y = f(x)$ is accomplished by a simple transconductor consisting of a differential amplifier. Its large signal transfer function is a smooth, sigmoid-like characteristic. A weak positive feedback is applied to increase the transconductance value without increasing the (W/L) ratio of the differential-pair transistors.

4.2. Current-Mode VLSI OCNN Neural Chip: Prototyping and Demonstration

To illustrate the implementation feasibility, a programmable 5x5 cellular neural processing chip

was designed, fabricated and tested in a scalable CMOS technology through MOSIS Services.

A circuit board was built to demonstrate the operation of this prototype chip. Experiments on edge detection were performed. The measured result agrees well with the C-based simulation result. The CPU time for the C-based simulation is 2.53 seconds. The speedup is about 160,000.

A OCNN chip of 128×128 annealed neurons has been under development and can be realized in a $1.5 \text{ cm} \times 1.5 \text{ cm}$ chip. A network of 1024×1024 annealed neurons is feasible to be designed with 64 128×128 OCNN chips and packaged into a 3-D die stack.

5 Smart Vision System-On-A-Chip Design

An low-power 1024×1024 -pixel APS integrated with a 1024×1024 neural processor through a smart window handler has been under development by using a 3-D VLSI die stacking technology combined with a sub-0.5-micron low power SOI CMOS process technology. A 3-D VLSI stack of dimensions $3 \text{ cm} \times 3 \text{ cm} \times 0.5 \text{ cm}$ is projected to accommodate a complete 1024×1024 -array neural. Figure 4 illustrated that a $5 \text{ cm} \times 10 \text{ cm}$ MCM is used to implement the smart vision system into a single packaged SOAC chip.

The neural processor operation speed is up to 4 MHz. The neural processor provides 4 tera-operations per second. The power dissipation of the smart vision MCM is about 1 W at 4 MHz nominal operation. Its volume is less than 100 cm^3 and its mass is about 200 gm. A miniaturized highly integrated vision system is therefore feasible to be implemented into a compact MCM at a manageable power dissipation rate.

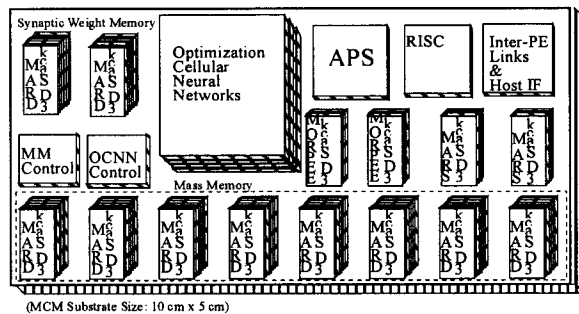


Fig. 4. A Smart Vision MCM Design.

6. Conclusion

Demonstration of the concept of the smart vision system based on APS integrated with programmable neural processor gives the feasibility of design the proposed system on a chip. This highly integrated and ultra-high-speed information processing smart vision system on-a-chip can be used on various NASA scientific missions and other industrial or commercial vision applications.

Acknowledgments

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